

ABSTRACT

A configuration circuit includes a latch and a dedicated non-volatile memory cell. The non-volatile memory cell is initially programmed or erased. The latch is then set to store a first logic value by coupling the latch to a first voltage supply terminal in response to an activated control signal. When the control signal is de-activated, the latch is de-coupled from the first voltage supply terminal and coupled to the non-volatile memory cell. If the non-volatile memory cell is programmed, the latch is coupled to a second voltage supply terminal, thereby storing a second logic value in the latch. If the non-volatile memory cell is erased, the latch is isolated from the second voltage supply terminal, and the first logic value remains stored in the latch. The latch can also be directly written through one or more access transistors, thereby facilitating testing.